Preliminary Hardware Design for A Silicon Vertex Trigger

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Introduction

This note is intended to document the preliminary hardware design that has been developed over the last several months. The original design appeared in the Silicon detector TDR and was done by myself and David Pellet of U.C./Davis.

This device is designed to take track roads created by the level 1 fiber trigger, select all the hits in the silicon detector that lie in these roads and send them to one of several Digital Signal Processors. Track data from the DSP's is sent directly to an MBT board in a concentrator crate in the CFT preprocessor crate.

The silicon device is naturally segmented in 30 degree sectors. This design is for 60 degree sectors and it is set up for 32 tracks per sector. The fiber tracker provides roads matched to the 60 degree sector. At present, they can provide up to 64 tracks per sector. (384 total tracks). Buss sizes in this design can handle up to 64 tracks but such a large number of tracks may lead to excessive processing times.

Studies by U. Heintz (ref. #) indicates that the physical overlap of the detectors is adequate to account for the track curvature. Thus, this design uses roads generated only in one 60 degree sector of the fiber tracker (no overlap with neighboring sectors).

This is a data driven design. Whenever there is data to process, it is processed and sent out. It relies completely on the front end system filling all of its buffers to halt data flow (other level 2 systems do the same). It also has only 16 buffers so buffer overflow is prevented by the front end buffers going completely full.

This report is organized as follows. The next section presents a block diagram of a crate and describes the overall operation. Following this, there is a more detailed description of each of the three modules. These sections should be sufficient to be the starting point for detailed engineering design.

System Overview

The trigger processor is divided up into 6 crates with each crate handling a 60 degree sector of silicon. The crates will be VME-64 VIPA crates that are similar to those used in the rest of the tracking system. This design also uses the special J3 back plane and the fiber optic receiver board designed for the tracking system.

Fig. 1 shows the overall block diagram of a silicon trigger crate. The portion at the upper left shows the input from the fiber trigger. This is the Fiber Road card. There is one of these cards per crate (SVT sector). The current design of the CFT concentrator cards creates 60 degree sectors to match the silicon system. Each 60 degree sector is sent over a single fiber optic cable to both the CFTpp and the SVT. Each CFT output consists of a list of the 32 highest PT tracks for that sector. The STT will preserve the order of these tracks and send its results to the CFTpp. The CFTpp will process the tracks that it receives directly from the CFT concentrator. As long as it maintains a map locating the position of each input track, it is simple to add the STT data when it arrives. The first track sent by the STT will be the same as the first track that the CFTpp received from the CFT concentrator and so on. Thus, the CFTpp can send to the global processor everything that the tracker knows about a track. In addition, the tracks can be sorted in Pt order.

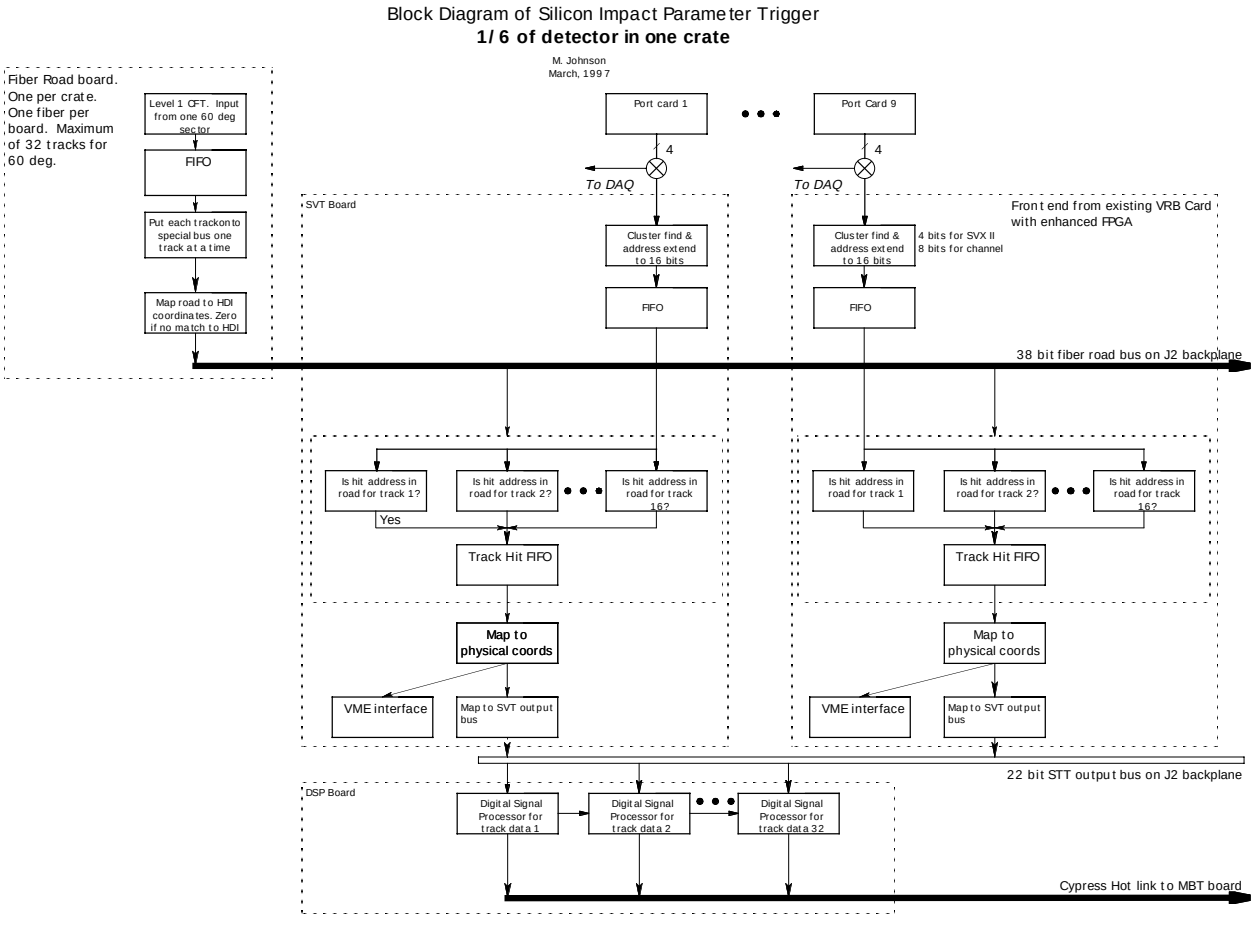

Figure 1

The top right part of figure 1 is the SVT trigger board. It is responsible for finding the centroid of SVX clusters and then selecting the centroids that lie within the fiber roads. The SVX data is obtained by passively splitting the fiber optic signals that are

sent to the VRB. Four of these cables are sent to each SVT card. Each silicon 30 degree sector uses 3 fiber optic cables so a 60 degree sector uses 6. Six barrels then require 36 cables and 9 SVT cards. Eight barrels require 12 cards. Since the input is identical to that arriving at a VRB, it is possible to use the same fiber receiver board that fits behind the VME back plane. Similarly, one can use the same J3 back plane. Note that the J3 back plane can house at most 12 fiber optic receivers so 8 barrels is the upper limit.

Data from the SVT trigger cards is sent over a special bus to a DSP card (Digital Signal Processor) which computes track parameters. This design uses one DSP per track and puts all 32 of them on one board. The DSP's can either be commercial processors of Field Programmable Gate Arrays programmed to do DSP functions. I prefer the latter since it provides the ability to implement special purpose functions. In either case it should be easy to get all of them on a single board.

Output of the DSP board is over a Cypress hot link to an MBT board in the CFTpp for transfer to the L2 global processor and possibly over VME to a VBD for transfer to level 3. All data is sent to the Global processor so it is possible to get all L3 from the global. Addition of L3 readout requires buffering the DSP card output and some additional buffer control from the crate controller. This is not hard to do but it is not included in this design. If needed, it can be copied from the tracking crate controller.

The VME interfaces to the Fiber Road card and the SVT Trigger are used only for parameter loading and diagnostics (mark and pass for example).

An important question in this design is where to put the de-randomizing buffers. This design is the same as the original which puts the buffers after the Field Programmable Gate Arrays in the SVT Trigger card. Everything upstream of this is in lock step and can keep up with level 1 triggers while the operations following the FPGA are not. This is also the point where the amount of information to buffer is smallest. Finally, this design eliminates the need for buffers in the Fiber Road card.

The start of the fiber road data from the CFT is delayed from the arrival of the L1 trigger. Fiber roads are now thought to be out in 2.4 μs but transfer across the buss between the Fiber Road card and the SVT trigger card is likely to take 2 to 3 μs. SVX digitization takes a little less than 3 μs. Thus, SVX data will start arriving before the roads are loaded into the FPGA's. This is OK because there is a FIFO at the receiver which can buffer up to one entire event. There will not be pileup because the current plan is to flush the SVX pipeline after every L1 trigger. This will provide an extra 4 μs before a new L1 trigger could arrive at the SVT.

Fiber Road Card

Fig 2 shows a block diagram of the Fiber Road card. It receives the fiber roads, translates them to silicon readout coordinates and then sends out the roads one at a

time over a dedicated bus to load the SVT cards. It also serves as the crate controller linking commands from the framework such as L1 accept to the rest of the crate and controlling the readout of the DSP board by the VBD. Since it is a crate controller, it must reside in slot 15 of the VIPA crate (if we use the present tracking J3 back plane). Note that the VBD is required to be in slot 4 if this backplane is used.

Fiber Road Card

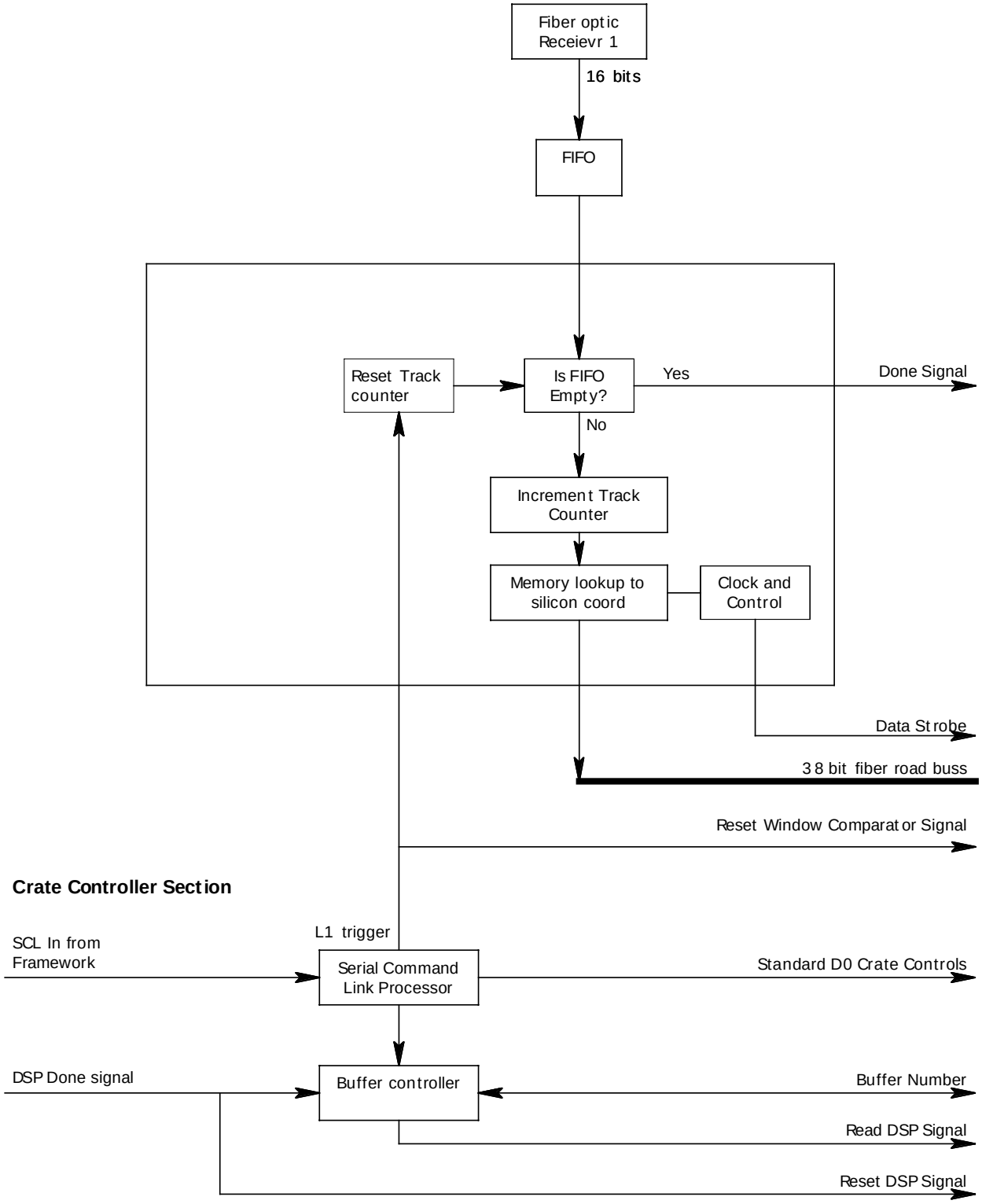

Figure 2

Data from the CFT are converted to electrical signals and stored in a FIFO. A FIFO is required to decouple the data sending clock (on the platform) from the local crate clock. This board also provides buffer control. This means that the board keeps a list of free pointers. Whenever an event is sent to the DSP board, the buffer is put back on the free buffer list. Whenever a new L1 accept occurs, a buffer is moved off the free list into the DSP list. It is assumed that it will never run out of buffers because the front end systems have only 16 buffers. If there are no free buffers, it is an error condition.

As mentioned above, there is no buffer provision for sending data to the L3 system. If this is required, additional L2 buffers will need to be provided on the DSP board. These will be controlled by this board using information (L2 accepts) from the trigger framework. Buffer control for this transfer occurs on dedicated lines on the J3 back plane. This is identical to the VRB control. The present J3 has only 12 slots connected to slot 15 for buffer control. If an 8 barrel silicon detector is made, then all 12 slots are used for the SVT trigger cards and there is no space for a DSP card. Then, if L3 readout is required, either the back plane needs to be re laid out to add one more slot (preferred solution) or one needs to use some of the other user defined pins for the DSP buffer control.

The range of roads that are processed in this silicon trigger crate are preloaded into a window comparator for each fiber. As the data is read out of the FIFO, it is checked to see if it is within the range. If not, the road is discarded. Conversion from CFT coordinates to Silicon coordinates is done via a look up memory just before the coordinate is put out onto the fiber road buss to the SVT. The 16 bit track code is used to look up the starting and ending address in each of the four silicon layers. Each silicon point is 16 bits so this operation generates 8 bytes of data. The bus to load the SVT cards is 38 bits wide so that the starting and ending address can be sent simultaneously. A six bit track number is appended to the two data points. This number runs from 0 to 31 and corresponds to the DSP that will process the track. The first road to arrive from the CFT is track 1 and so on.

The buss structure of the fiber road buss is similar to that used by the data cables for the L2 trigger in the first run of D0. Each silicon filter element in the SVT card is analogous to a dual port memory and processor node in the old L2 system. Each filter element knows the range of silicon addresses that it is responsible for. It looks at the bus for the starting silicon address. If it is within its range, it strobes the data into its memory. Otherwise, it does nothing. Note that every SVT filter could load a give fiber road point; there are no restrictions. The road translation memory is set up so that if the starting address is in the filter range, the trailing address will be also so only the leading edge need be checked. This structure has several advantages. The bus is very simple; only the data and a data strobe are required. There is no bus arbitration or handshaking. The bus can easily be extended to a second crate with at most a repeater. The details of the mapping can be easily changed; only the mapping memory and the range codes in each filter need be modified.

The buss would need 38 signal and one strobe (plus some number of grounds). Since there is no handshaking, the bus can run at 25 ns/cycle. Four cycles are needed per road. Assuming 32 tracks per trigger sector, this takes 3.2 μs which is over the SVX digitization time. Note that cluster finding will add perhaps 100 ns to the digitization and settling time. The Fiber road card provides a Done signal which is used to start the SVT trigger card processing.

It may also be possible to run the buss at 18.8 ns cycle time which would reduce the time to send 32 tracks to 2.4 μs. With current FPGA's, running the buss at 18.8 ns would result in a marginal design because the data set up times would be too short.

The only use of VME on this card is to load parameters such as the ranges for the fiber roads and for diagnostics. There is a mark and pass mode where data sent over the fiber road buss is also put into a buffer memory that can be read over VME. This section is not shown in figure 2.

SVT Trigger board

Figure 3 shows a block diagram of the SVT trigger board. This board has a front end that is identical to the VRB's. It uses the same VTM receiver module that is used by the VRB. The VTM is a medium sized board that is located behind the VME crate and converts optical signals to electrical. The raw silicon hits from the SVX are optically split and stored in FIFO's - one for each fiber. The output of each FIFO is fed into a Field Programmable Gate Array which provide bookkeeping (detecting an end-of-record for example) and some limited data processing. The mean position of silicon clusters is computed here. Output of the FPGA is to a 16 deep de randomizing buffer for L2. If the buffer is moved to after the filter FPGA, then the design is altered as follows. If the fiber roads delayed beyond SVX digitization time, data will be held in the input FIFO until the roads are complete. Since the FPGA calculates cluster centers, there will not be an output point at every clock cycle. Therefore, the FPGA will put out a null code (address outside of any road) when there is no data point. The downstream electronics is synchronous so it does an operation every clock cycle. However, since the null code is simply an address outside of any window, it is automatically ignored.

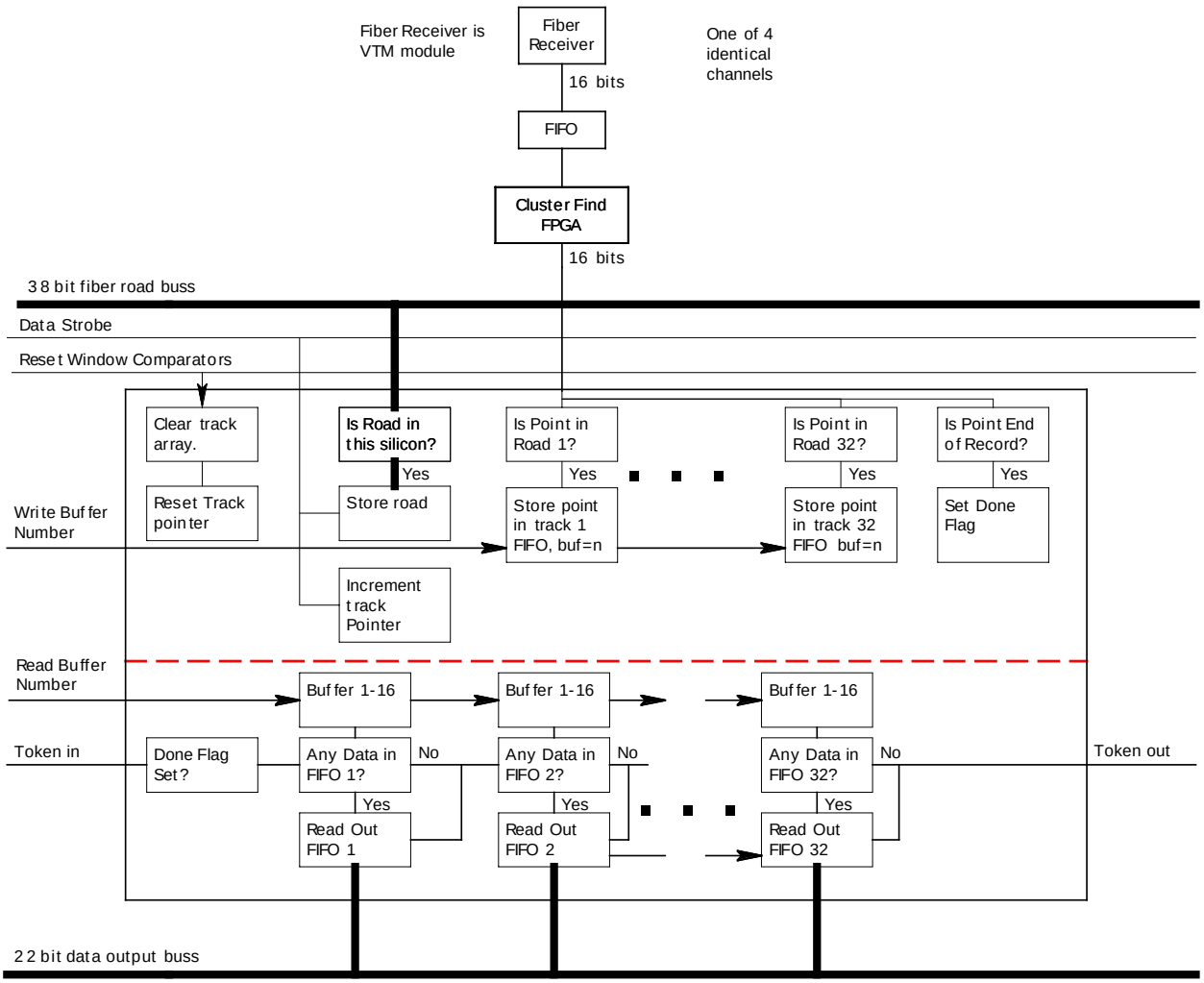

Figure 3

The VRB system has an end-of-record code so this will be passed through the cluster finder and used to indicate that all the data from a given fiber optic cable has been processed. The individual done flags are ANDed together to indicate that an SVT board has finished an event. The board DONE flags are ANDed together on the Fiber road card to indicate that an event has been completely read in and processed. This is used to increment the buffer pointer for the next event. A non zero buffer count is used to initiate shipping data to the DSP board.

The output of the cluster finder is 16 bits. The cluster finder will add 2 bits (12.5 micron resolution). The chip ID has 6 bits allocated in the upper byte of the chip ID and there are 7 bits of channel number. There are no more than 9 chips in a silicon HDI string so we can reduce the 6 bit chip ID to 5 and also use the extra bit in the channel number byte. Thus the channel number occupies the lower 9 bits (2 added

fractional channel bits) and the chip occupies the next 5 bits. The upper 2 bits are used for special codes such end-of-record.

The filter is implemented in an FPGA and is quite straight forward. It consists of 32 window comparators, each 16 bits wide. Each SVX data point will be simultaneously compared with all 32 windows. If it is within one or more windows, it will be entered onto the output FIFO for those tracks. All comparators and FIFO's are independent so it is possible for a given point to be in all 32 windows. The data point is stored in the FIFO according to the track number that was sent along with the fiber road. Note that each readout fiber has 2 HDI's on it (2 pieces of silicon). If the silicon to fiber optic mapping is unfavorable, it is possible for a given readout fiber to have 2 points for a given road. If this occurs, one may need to have 64 window comparators per FPGA so that a given road could have 2 different windows per optical fiber.

The points found in the roads need to go to two places. In normal running, the data is sent to a DSP board. For diagnostics (mark and pass) they are read out over normal VME via a VBD as well. The transfer to the DSP needs to be on a special buss because the output of the DSP's may be sent to L3 via a VBD which uses the VME buss. These need to be separate since one event could be reading out to L3 while another is being sent to the DSP's. Doing both over VME would significantly slow down the trigger. This buss is also similar to the data cables used in the first run of D0. Here the DSP chips correspond to L2 nodes and the filter FPGA's to front end crates. For the Fiber Road card a token was not required since there was only one source and multiple destinations. In this case there are multiple sources and (possibly) multiple destinations so a token is required. The D0 system for run 1 was constantly circulating the token around all possible transmitters. This is not the best way to operate this system. A token requires 2 clock cycles to move from one filter FPGA to the next. This is one cycle to receive and one to transmit. There are a minimum of 36 filters in a crate so it takes 72 cycles for each pass. Thirty two tracks at 4 points per track is only 128 cycles so passing the token twice around the loop takes more time than sending the data! An 'ORed' Done signal is provided which will signal the completion of all filters. At this point the Fiber Road card issues a token to the first filter section. This section keeps the token until it is done sending out its data and then it passes the token on to the next filter.

DSP Board

This board fits tracks to the points found in the roads. A block diagram is shown in fig. 4. The method used is the linearized chi squared method as described in CDF note ##. This fit requires only a sum-of-products which is well suited for digital signal processors. The processors could be general purpose chips or FPGA's coded to emulate DSP's. The latter programming is available commercially for several FPGA's. The main advantage of using FPGA's is that the algorithm can be expanded so that several operations can be done in parallel. For example, in computing a chi square, one needs to do the sum of 4 products. In an FPGA, all 4 products can be

computed in parallel at one step, the second step would sum together 2 pairs in parallel and the third step would compute the final sum. Depending on the precision required in the multiply, this might be able to be done less than 100 ns. Such high speed would be very useful if there were a lot of points in a road. One could simply compute all possible combinations and take the lowest chi squared.

Data from the SVT card contains the point and the five bit track number (21 bits total). Each DSP has been preassigned to a track number so it will monitor the track number and load in the data for its assigned track. Again, there is no handshaking on this bus. When the SVT token is received back at the Fiber Road card indicating that the data transfer is complete, a signal is sent to the DSP's to start them computing. Each DSP raises a DSP done line when it is finished. When all DSP's are finished, event readout to the CFTpp commences.

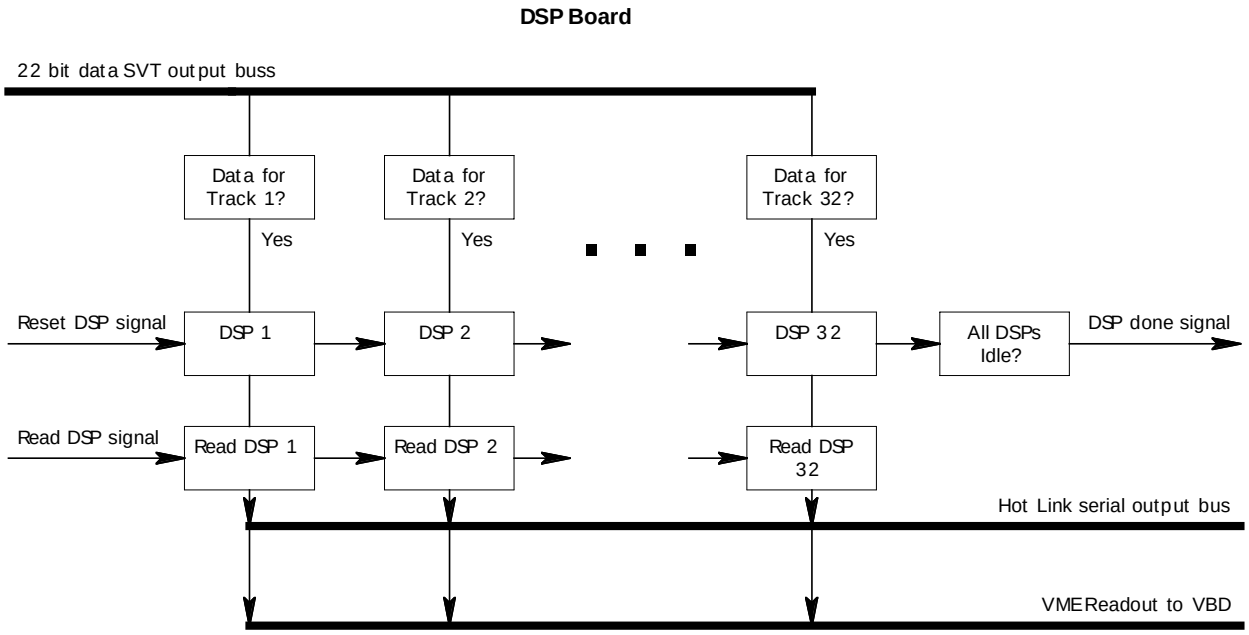

Figure 3

The readout to the CFTpp is over a Cypress hotlink to an MBT card in the CFTpp crate. There is one Hot Link per DSP card. Readout is sequential starting with DSP 1. Tracks are loaded in order so for n tracks, it will read out n DSP's. Data does not include the fiber road number but it would be trivial to add. Since the DSP's are read out in numerical order and DSP 1 always has track 1, the data order should be identical to the order that the tracks were received in. This means that the work to associate the SVT data with the CFT tracks in the L2 CFTpp is minimized.

There are 7 or 8 inputs to an MBT board. If there is one DSP board per crate, all six crates for the trigger can feed into one MBT.

If required, VME readout of the input and/or output of the DSP's is straight forward. The VBD requires block transfers so each of the DSP's arrays on a board

will need to compute the number of entries in its buffer. If the input data is required (for mark and pass), it is added to the buffer. These n numbers will then be summed to provide a total word count from the board which will be read by the VBD. Logic on the DSP board will string all the buffers together so that everything is read out in one VME block transfer. Each DSP board in the crate will have one block transfer.

Since readout to L3 is buffered by 8 buffers in the rest of D0, these boards will also require 8 buffers. The simplest scheme is to stack the data up in front of the VME buss controller. That is, data is put together as above but put into a buffer if VME is currently busy. Event number headers need to be added so the crate controller will have a bit more work to do. It is very similar to several other D0 systems.

Crate Structure

As mentioned above, this design uses a VME 64 VIPA crate. The auxiliary card cage in back is used to house the fiber optic receivers (VTM cards) for the SVT cards. The tracking J3 back plane is used which requires the crate controller in slot 15 and the VBD in slot 4. Fiber input to the Fiber Road card (which is also the crate controller) is via a fiber optic line into the front panel. The Serial Command Link also comes in the front panel of this card. The Cypress hot link the MBT card comes out of the front panel of the DSP.

If 8 barrel segments are needed and readout via the VBD to L3 is required, then the current J3 back plane needs to be modified to add one more slot since all 12 slots would be used for SVT cards and there would be no buffer control (for L3 readout) available to the DSP. If there is only one DSP card, it might be possible to put buffer control on the card and send a small amount of L2 data over the J2 back plane. This depends on the number of processors.

There are two special busses required in this design; the 38 bit Fiber Road buss and the 22 bit SVT output buss. There are 64 user definable , bussed lines on J2 of the VIPA back plane. This scheme uses 60 of these lines. Two additional done lines are needed leaving 2 spares. It may also be possible to reduce the size of the busses by a bit or two.